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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/641,700	08/15/2003	Jon S. Martens	ANRI-08064US1	9974

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FLIESLER MEYER, LLP
FOUR EMBARCADERO CENTER
SUITE 400
SAN FRANCISCO, CA 94111

EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/641,700	MARTENS ET AL.	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 21-25 is/are allowed.

6)☒ Claim(s) 1-9,11-13,15 and 16 is/are rejected.

7)☒ Claim(s) 10,14 and 17-20 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08/15/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 08/15/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 08/15/2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because reference number 9 and reference number 26 do not have date. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 6-7, 8, 11 are rejected under 35 U.S.C. 103(a) as obvious over Chodora (USP 6,147,501).

Regarding claim 1, Chodora teaches a method for efficiently characterizing an N-port device under test (DUT) (23) using a vector network analyzer (VNA) (21), wherein N is 2 or greater (Fig.1), the method including: (a)

dividing the N-port DUT (23) into multiple sub-devices (22) that each include less than N ports; (b) performing at least an M-port VNA calibration (Abstract, lines 2-5), where M is equal to a number of ports on the one of the multiple sub-devices (31, 32, 33, 34... Col.5, lines 42-53) having the greatest number of ports (28, 29).

Regarding claim 2, Chodora teach step (a) includes dividing the N-port DUT (23) into multiple sub-devices (31, 32, 33, 34... Col.5, lines 42-53) based on transmission path levels between the N-ports (e.g. Col.3, lines 57-66, Col.6, lines 55-62).

Regarding claim 6, Chodora teaches performing an M port calibration (Abstract).

Regarding claim 7, Chodora teaches the sub-devices (22) can include M ports (28, 29)(Fig.1).

Regarding claim 8, Chodora teaches performing an N port calibration (Abstract).

Regarding claim 11, Chodora teaches step (a) can be performed by a user with or without the assistance of the VNA, or by the VNA with or without the assistance of a user (e.g. Col.4, lines 42-47).

Chodora does not teach determine S-parameters for each sub-device. Chodora, however, disclose in figure 3, lines 81, 82 represents the lines from paragraph [0005] of current application that the signal is leaving and the signal is being injected into ports. It would obvious to one of ordinary skill in the art at the time the invention was made to include lines 81, 82 represents the lines from

paragraph [0005] of summary of the current application that the signal is leaving and the signal is being injected into ports is considered substitute as claimed.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chodora (USP 6,147,501) in view of Blackham (USP 6,188,968).

Regarding claim 9, Chodora fails to teach measuring S-parameters for the sub-device; and removing calibration errors from the measured S-parameters, the calibration errors determined by the VNA.

Blackham teaches measuring S-parameters for the sub-device (e.g. Col.5, lines 41-62); and removing calibration errors from the measured S-parameters, the calibration errors determined by the VNA (Abstract, lines 5-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include steps of measuring S-parameters for the sub-device; and removing calibration errors from the measured S-parameters, the calibration errors determined by the VNA as taught by Blackham in a method for efficiently characterizing an N-port device under test (DUT) using a vector network analyzer (VNA) of Chodora for the purpose of providing removing effects of adapters present during vector network analyzer calibration.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chodora (USP 6,147,501) in view of Bradley et al. (USP 5,524,281).

Regarding claim 12, Chodora teaches a method to be performed with a vector network analyzer (VNA) (21)(Abstract, lines 2-5), the method for efficiently characterizing an N-port device under test (DUT) (23), wherein N is 2 or greater, and wherein the N-port DUT is capable of being treated as multiple sub-devices

(22) that each include less than N ports, the method including: (a) performing at least an M-port VNA calibration (Abstract, lines 2-5), where M is equal to a number of ports on the one of the multiple sub-devices (31, 32, 33, 34,..., Col.5, lines 42-53) having the greatest number of ports (28, 29).

Chodora fails to disclose (b) presenting at least one menu that allows selection of which S-parameters are of interest for each sub-device; (c) accepting inputs that specify which S-parameters are of interest for each sub-device; and (d) determining the S-parameters of interest for each sub-device as identified at step (c), without determining the S-parameters that are not of interest.

Bradley et al. teach a menu that allows selection of which S-parameters are of interest for each sub-device (e.g. Col.106, lines 15-35); accepting inputs that specify which S-parameters are of interest for each sub-device (e.g. Col.106, lines 15-35); and determining the S-parameters of interest for each sub-device, without determining the S-parameters that are not of interest (e.g. Col.106, lines 15-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include steps of (b) presenting at least one menu that allows selection of which S-parameters are of interest for each sub-device; (c) accepting inputs that specify which S-parameters are of interest for each sub-device; and (d) determining the S-parameters of interest for each sub-device as identified at step (c), without determining the S-parameters that are not of interest as taught by Bradley et al. in a method for efficiently characterizing an N-port

device under test (DUT) using a vector network analyzer (VNA) of Chodora for the purpose of providing a network analyzer operation manual (Col.97, lines 16-20).

Regarding claim 13, Bradley et al. teach step of accepting the inputs from a user or a test controller (e.g. Col.11, lines 13-15).

Regarding claim 15, Bradley et al. teach the at least one menu includes a menu that allows selection of any possible combination of the S-parameters corresponding to a sub-device (Col.97, lines 16-20).

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chodora (USP 6,147,501) in view of Bradley et al. (USP 5,524,281) as applied to claim 12 above, and further in view of Blackham (USP 6,188,968).

Regarding claim 16, the combination of Chodora and Bradley et al. discussed supra, discloses the claimed invention except steps measuring the S-parameters of interest for each sub-device; and removing calibration errors from the measured S-parameters, the calibration errors determined by the VNA.

Blackham teaches steps of measuring the S-parameters of interest for each sub-device (e.g. Col.5, lines 41-62); and removing calibration errors from the measured S-parameters, the calibration errors determined by the VNA (Abstract, lines 5-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include steps of measuring S-parameters for the sub-device; and removing calibration errors from the measured S-parameters, the calibration errors determined by the VNA as taught by Blackham in a method for

efficiently characterizing an N-port device under test (DUT) using a vector network analyzer (VNA) of Chodora in view Bradley et al. of for the purpose of providing removing effects of adapters present during vector network analyzer calibration.

Other Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Blackham et al. (USP 6,836,743) disclose a method and a vector network analyzer compensate for unequal source match and load match of a test port of the vector network analyzer.

Dunsmore (USP 6,643,597) discloses a method and system for calibrating a test system and a vector network analyzer use models of unknown calibration standards for a standards-based calibration.

Blackham et al. (USP 6,060,888) disclose error correction method for reflection measurements of reciprocal devices in vector network analyzers.

Allowable Subject Matter

8. Claims 21-25 are allowed.

9. Claims 10, 14, 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

January 7, 2005

John Barlow
Supervisory Patent Examiner
Technology Center 2800